IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of

Divakaruni, et al

Serial No.: 09/718,850 Group Art Unit: 2811

Filed: November 22, 2000 Examiner: G. Munson

For: LOGIC SOI STRUCTURE, PROCESS AND APPLICATION FOR VERTICAL BIPOLAR TRANSISTOR

Assistant Commissioner of Patents
Washington, D.C. 20231

SUBMISSION OF PROPOSED DRAWING CORRECTIONS

Sir:

Submitted herewith are proposed drawing corrections, marked in red, to Figures 3 and 4. If approved, such corrections will be incorporated into the formal drawings at the time of allowance.

Approval and acknowledgment of receipt are respectfully requested.

Respectfully Submitted,

Frederick W. Gibb, III
Reg. No. 37,629

Date: 4/22/03

McGinn & Gibb, PLLC
2568-A Riva Road
Suite 304
Annapolis, MD 21401
Customer No. 29154

Certificate of Mailing

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail, postage prepaid, in an envelope addressed to the Assistant Commissioner for Patents, Washington, DC 20231 on April 22, 2003.

Frederick W. Gibb, III